REMARKS

Claims 1, 3-18, and 20-47 are pending in the present application. Claims 1, 3, and 16 have been rejected under § 103 as being unpatentable over Bell (US 5,642,075) (Bell) in view of Blake (US 6,847,904) (Blake). Claims 1-14, 16-27, and 38-47 have been rejected under § 103 as being unpatentable over Lee (US 2003/0152056) (Lee) in view of Lin (US 2004/0038701) (Lin) and Blake. Claims 15 and 28 have been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Yu et al. (US 5,365,190) (Yu). Claims 29-37 have been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Gunzelmann et al (US 2004/0097250) (Gunzelmann).

The dependency of claim 2 has been amended so as not to depend from canceled claim 2.

Independent claim 1 has been rejected under § 103 as being unpatentable over Bell in view of Blake. Claim 1 has also been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake.

Amended claim 1 recites an RF apparatus formed using an integrated circuit comprising "power amplifier circuitry formed using the integrated circuit," "a digital interface for providing an interface between the integrated circuit and an external controller, wherein the digital interface is a digital interface for receiving a digital signal from the external controller, and wherein the digital signal contains power control data," and "circuitry formed using the integrated circuit for generating a power ramp profile to vary the output power of the RF power amplifier based on a desired output power level relating to the digital signal from the external controller."

Bell discloses an amplifier circuit using an automatic gain control (AGC). The circuit of Bell is designed to adjust the gain of amplifier 14 so that the output Vout is maintained at a desired RMS value. Bell uses a reference voltage Vref to maintain the RMS value of Vout. In the

example provided, Bell states that 2Vref is equal to 2 Volts. (Col. 3, line 61). Blake discloses a programmable gain amplifier. Blake discloses an external analog reference voltage Vref that is connected to a gain setting resistor ladder network 112. Applicant asserts that, in both Bell and Blake, Vref is not a digital signal. Vref in both patents is described as a voltage reference. One typical definition of a voltage reference is a fixed/constant voltage irrespective of the loading of a device, power variation, and temperature. This is different from a digital signal, which is a signal in which discrete steps are used to represent information, commonly using binary codes (1's and 0's). Further, Bell even teaches that Vref can be proportionally reduced to compensate for loss. It is unclear how a digital signal can be proportionally reduced, if it can only have a "high" or "low" value. Applicants request that the Examiner explain how the reference voltages in Bell and Blake are digital signals.

As discussed above, amended claim 1 recites a power amplifier formed using the integrated circuit, circuitry for generating a power ramp profile formed using the integrated circuit, and a digital interface for providing an interface between the integrated circuit and an external controller. As argued above, Applicants assert that the voltage references (Vref) are not digital interfaces. The Office Action also relies on logical circuits in Figs. 6A and 6B of Bell as digital interfaces, and ramp generator 24. However, claim 1 recites that the digital interface provides an interface between the integrated circuit and an external controller. Using the Office Action's interpretation of Bell, the logical circuits in FIGS. 6A and 6B do not appear to provide an interface with an external controller, since the ramp generator and power amplifier would be formed using the same integrated circuit. FIGS. 6A and 6B of Bell show the gain latch, ripple counter, delay and reset control circuitry shown in FIG. 1. It is unclear how these could be an interface that meets the requirements of amended claim 1.

Lee discloses a wireless local area network (WLAN) transceiving integrated circuit (IC), including a WLAN interface, an input buffer and controller, and a processor. An IC of Lee (e.g., IC 350 of FIG. 3B) includes a power amplifier 352, core components 351, and serial and parallel interfaces 320 and 324 to interface with a host 322. An IC of Lee (e.g., IC 400 of FIG. 4A) may include a baseband 404. Lee does not appear to teach or suggest, however, an integrated circuit with a digital interface for providing an interface between the integrated circuit and an external controller, wherein the digital interface is a digital interface for receiving a digital signal from an external controller, and wherein the digital signal contains power control data. The interface between the power amplifier 352 and the core components 351 (FIG. 3B) appears to include an transmit signal TX and an non-digital power control signal TX_PC. There also appears to be no teaching in Lee that the interfaces 320 and 324 (FIG. 3B) provide an interface for a digital signal that contains power control data.

Lin discloses a wireless transmission apparatus used for transmitting an RF signal. Like Lee, Lin also does not teach or suggest an integrated circuit with a digital interface for providing an interface between the integrated circuit and an external controller, wherein the digital interface is a digital interface for receiving a digital signal from the external controller, and wherein the digital signal contains power control data. The power amplifier 118 receives an RF input signal R118 and an analog control signal from the power control loop 116.

For at least these reasons, applicant asserts that amended claim 1 is allowable over the cited prior art. Since dependent claims 3-17 depend from amended claim 1, it is also believed that these claims are allowable over the prior art.

Claim 18 recites a method of amplifying RF signals comprising "providing an RF power amplifier formed on an integrated circuit," "storing a plurality of ramp profiles in the integrated

circuit," "receiving one or more digital control signals containing power control data from a controller that is external to the integrated circuit, wherein the control signals are received over a digital interface," and "selecting one of the ramp profiles to vary the output power of the RF power amplifier based on a desired output power level relating to one or more of the digital control signals from the controller."

When rejecting claim 18, the Office Action states that "Lin discloses a plurality of stored ramp profiles and a selection as claimed (see [0018])." However, Lin does not teach or suggest storing the ramp profiles on an integrated circuit, and receiving digital control signals containing power control data from a controller that is external to the integrated circuit.

For this reason, and for reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 18 is allowable over the prior art. Since dependent claims 20-28 depend from amended claim 18, it is also believed that these claims are allowable over the prior art.

Amended claim 38 recites an RF power amplifier module comprising "power amplifier circuitry formed using a first integrated circuit," "control circuitry formed using a second integrated circuit," "a digital interface formed using the first integrated circuit, wherein the digital interface is configured to allow digital power control signals from an external controller to be received by the power amplifier circuitry," and "memory formed using one of the first and second integrated circuits, wherein a plurality of ramp profiles are stored in the memory for varying the output power of the power amplifier circuitry based on desired output power levels relating to one or more of the digital power control signals received from the external controller."

When rejecting claim 38, the Office Action states that claim 38 is rejected for the same reason as claim 1, "wherein the 'on-chip' amplifier would read on the 'first integrated circuit', the

'WLAN transceiving integrated circuit' for controlling amplifier power would read on the 'second integrated circuit' (see [045], [0049])." Using this interpretation of FIG. 3A of Lee, the power control signal TX_PC would have to be the "digital power control signal." Applicant can find no evidence in Lee that the power control signal TX_PC is a digital signal. Also, when Lee describes other interfaces in FIG. 3A that are digital interfaces (interface 320, 324, 308, etc.), Lee explicitly does so. This is appears to be further evidence that signal TX_PC is not a digital signal.

For these reasons, and for the reasons set forth above with respect to amended claim 1, applicant asserts that amended claim 38 is allowable over the prior art. Since dependent claims 39-47 depend from amended claim 38, it is also believed that these claims are allowable over the prior art.

Claim 29 recites a method of controlling a wireless communication device comprising "providing a baseband controller," "providing an integrated circuit having an RF power amplifier, memory, a digital interface, and an RF input, all formed using the integrated circuit," "storing a plurality of ramp profiles in the memory formed using the integrated circuit," "sending a digital power control signal from the baseband controller to the integrated circuit using the digital interface, wherein the digital power control signal relates to a desired output power level," "selecting one of the plurality of ramp profiles based on the digital power control signal received from the baseband controller," and "using the selected ramp profile to control the output power of the RF power amplifier."

As mentioned above, claim 29 has been rejected under § 103 as being unpatentable over Lee in view of Lin and Blake, and further in view of Gunzelmann. Lee, Lin, and Blake are discussed above. Gunzelmann discloses a transmission configuration for a mobile radio communication system. Gunzelmann shows an interface 2 that includes conductors 21, 22, 23,

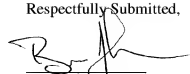
and 24. Conductor 21 carries a digital signal and is designed for transmission of the payload data which is provided from a digital signal processor. The module 3 (including the power amplifier 31) of Gunzelmann does not appear to receive an analog RF input signal to be amplified, but rather appears to receive a digital signal, which is converted into a signal to be amplified. Further, a combination of the cited references does not teach or suggest a method as recited in claim 29. For example, such a combination does not teach or suggest providing an integrated circuit having an RF power amplifier, memory, a digital interface, and sending a digital power control signal from the baseband controller to the integrated circuit using the digital interface.

For at least these reasons, and for reasons set forth above with respect to the other claims, applicant asserts that amended claim 29 is allowable over the prior art. Since dependent claims 39-47 depend from amended claim 29, it is also believed that these claims are allowable over the prior art.

It is respectfully submitted that all claims are patentable over the prior art. It is further more respectfully submitted that all other matters have been addressed and remedied and that the application is in form for allowance. Should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Bruce A. Johnson, Applicants' Attorney at 512-301-9900 so that such issues may be resolved as expeditiously as possible. Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 to deposit

account number 50-3864 (Johnson & Associates).

Respectfully Submitted,



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Date

Bruce A. Johnson
Reg. No. 37361
Attorney for Applicant(s)

Customer Number 30163
Bruce A. Johnson
Johnson & Associates
PO Box 90698
Austin, TX 78709-0698
Tel. 512-301-9900
Fax 512-301-9915